JP60048617A2:SIGNAL SELECTING CIRCUIT

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Country
Kind
Inventor(s)
Applicant(s)
Issued/Filed Dates
Application Number
IPC Class
Abstract

Family
Other Abstract Info
Foreign References

JP Japan

WADA TAKAMICHI
UNO TADASHI
SAITO MASAYOSHI
MIZUSHIMA YOKO

MATSUSHITA ELECTRIC IND CO LTD
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H03K 23/66;

Purpose: To allow the frequency division of 2N and (2N+1) to be executed surely by applying two kinds of pulses opposite in phase to one input terminal and a control signal for switching a frequency-dividing value to the other input terminal.
Constitution: Signals b, c opposite in phase are applied to terminals 24, 25 and the control signal (h) for switching frequency dividing value is applied to a terminal 32. If there is a delay in a time t1 in which the signal (h) is changed and the t1 is invaded between times t2 and t3, an output k' of an NAND gate 35 is kept to "1" till the time t3 and an output j' of an NAND gate 34 goes to "1" from the time t1, then a period T4 (t1¡ t3) where both logical levels go to "1" is produced. That is, an output (d) of an NOR gate 6 is also at "0" during this period. Thus, the frequency dividing operation of 2N and (2N+1) is executed correctly without causing the change in the logical level of an output (d).

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